Monte Carlo Yield Analysis Using MMICAD

Yield analysis is defined as the forecasting of the production yield of a simulated circuit.

To accomplish this goal, a circuit designer must specify:

I. The performance criteria to be used when the simulator is assessing YIELD.
II. The tolerances to be placed on circuit variables.
III. The number of trials (simulations).

Each of these criteria will be discussed in the following sections.

I. Yield Performance (Optimization)

In MMICAD the OPT block is used to specify the criteria for passing or rejecting a simulated circuit response. This simulation is considered to have PASSED if the cumulative error function is equal to 0 or, if ETERM is specified, the cumulative error is less than the value placed in the ETERM statement.

```
OPT
 LNA dB [S21] LT 15
 LNA dB [S21] GT 14
 LNA dB [NF] LT 2
```

For example, the network LNA will **PASS** if the gain response is between 14 and 15 dB with the noise figure simultaneously less than 2 dB. If this is so, the cumulative error function will be equal to zero.

```
OPT
 ETERM=15
 LNA dB [NF] EQ 2
 LNA dB [S21] EQ 15
```

For example, the network LNA will **PASS** when the noise figure and gain are equal to 2 dB and 15 dB respectively. Since this condition will never be precisely met over the entire frequency range, the ETERM statement is used to specify the error function below which the circuit is considered to have **PASSED**. In the above example, the network LNA will only be considered to have **PASSED** when the cumulative error function falls below 15.

II. Variable Tolerancing

Since the OPT block is used to specify the yield criteria for the simulation, variables can be toleranced using any of the two standard MMICAD formats (%, or ?). However, a variable specified with these formats will assume a flat distribution for the Monte Carlo sampling.

Often, however, the user is interested in specifying a normal distribution for a variable for the Monte Carlo sampling. To accommodate this, the following syntax is supported:

<variable> = $ <data1> <data2> $

where	<variable>	is a VAR block variable
	$	indicates a normal distribution
	<data1>	is the value of the variable at the peak of the normal distribution
	<data2>	is the delta in the variable at one standard deviation

As with the "?" and "%" syntax, in-line assignments may also be made in the CKT block (i.e. RES=1 2 R=$ 100 10 $)

Example:

```
VAR
 RSQ = $ 55 5 $
```

In this case, the variable RSQ will be assumed to have a normal distribution with a peak of 55 ohms and this first standard deviation occurring at 50 and 60 ohms.

III. Setting the Number of Trials

This is specified in the PARAM block using the normal syntax.

Example:

```
PARAM
 SWEEP 1 500 1
```

This would specify 500 trials during yield analysis.

Performing a Yield Analysis

After the yield goals are specified, the pertinent circuit variables toleranced and the number of trials specified, the designer is ready to perform a yield analysis. MMICAD allows the user to specify three different modes for yield analysis, as follows:

(1) mode **YIELD** (display all trials)
(2) mode **YIELDP** (display only PASS trials)
(3) mode **YIELDF** (display only FAIL trials)

The yield analysis is then conducted by selecting "Variational Analysis" from the "RUN" menu. After the user selects the FRAME to view, the response is plotted on the screen, (according to the mode setting above).

An indication of the trial, % yield, the number passed and the number failed, will be displayed along with the FRAME.

At the completion of the MONTE CARLO Yield Analysis, the display will indicate a tabular result for the first 8 variables selected for tolerancing as follows:

TRIAL P/F <name1> <name2> ...... <name8>

(The P/F column indicates PASS or FAIL.)

Mode Yield Results:

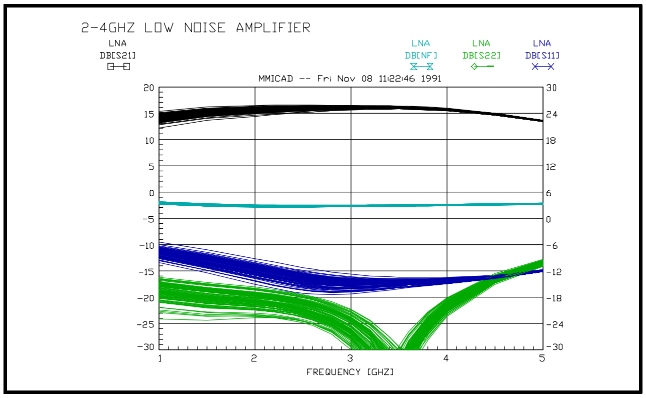

Figure 1 YIELD Circuit Responses

MMICAD Yield Analysis

TRIAL		RSQ1	RSQ2	CSQ
1	F	56.446	110.62	259.50
2	F	48.940	109.63	306.81
3	P	48.795	100.96	280.34
4	F	52.413	111.46	315.56
5	F	44.962	81.921	272.66
6	F	39.758	102.93	297.56
7	P	51.992	103.53	286.19
8	P	43.852	94.173	306.00
9	P	49.649	92.200	301.28
10	F	54.762	105.80	295.76
11	F	46.778	110.14	289.60
12	P	48.748	103.57	315.71
13	F	48.724	107.38	317.44
14	F	43.474	106.65	332.28
15	P	50.200	90.258	339.48
16	P	52.450	89.557	290.92
17	P	43.935	90.636	293.51
18	P	52.868	99.774	330.05
19	P	59.205	93.570	319.25
20	P	59.086	95.693	257.99
21	P	47.502	96.823	313.04
22	P	45.534	104.44	282.28
23	P	45.982	91.936	289.93
24	P	43.102	95.034	285.39
25	P	52.293	92.912	297.47
26	P	43.132	101.39	296.82
27	P	43.014	86.497	326.92
28	F	48.108	105.48	339.80
29	F	47.290	115.79	275.95
30	P	46.624	93.797	305.78
31	F	46.088	105.61	276.10
32	F	49.591	114.09	257.06
33	P	48.115	101.28	322.90
34	P	51.992	105.51	303.00
35	F	47.473	110.11	325.47
36	F	49.704	110.20	256.63
37	F	55.276	113.92	319.90
38	F	59.715	121.35	273.48
39	F	48.484	112.51	289.38
40	P	49.326	98.707	236.05
41	P	49.109	86.442	289.95
42	P	48.796	104.30	295.93
43	P	47.225	102.75	327.35
44	F	55.624	106.28	322.56
45	P	48.851	93.963	310.21
46	P	49.878	106.61	294.81
47	F	53.430	110.50	290.66
48	F	43.536	114.60	293.25
49	P	54.651	83.639	306.16
50	F	48.104	107.02	337.28
51	P	52.630	82.847	307.78
52	F	41.101	114.66	311.38
53	F	54.561	107.93	301.72
54	F	48.220	108.08	323.15
55	P	52.482	91.980	325.30
56	P	45.454	99.216	283.07
57	F	55.037	116.11	278.56
58	P	53.374	89.712	281.83
59	P	46.083	92.996	291.24
60	F	58.775	96.209	331.64
61	P	45.075	98.557	287.15
62	P	42.939	99.405	313.30
63	P	44.379	98.415	276.55
64	P	50.057	100.19	309.32
65	F	48.380	107.76	272.55
66	F	59.443	82.599	283.03
67	F	53.499	119.79	265.07
68	P	48.294	83.826	283.52
69	P	51.113	94.360	283.26
70	F	39.999	124.41	324.38
71	P	46.310	97.852	277.74
72	F	55.818	117.30	309.95
73	F	45.811	111.82	274.94
74	P	50.816	91.614	310.60
75	F	54.461	107.84	289.39
76	P	57.740	92.166	355.17
77	P	54.460	97.549	289.23
78	P	52.446	92.139	317.08
79	P	45.162	91.282	295.51
80	P	57.212	90.559	308.33
81	P	55.374	99.089	316.17
82	F	41.270	101.20	300.91
83	P	50.812	101.49	294.68
84	P	43.833	99.325	305.32
85	F	48.888	110.30	308.79
86	P	45.980	89.729	304.65
87	P	53.816	97.647	333.21
88	P	47.202	95.012	308.29
89	P	45.174	104.27	299.49
90	F	53.210	118.42	262.00
91	P	47.284	88.281	259.28
92	F	47.680	107.10	281.04
93	F	38.094	84.988	290.07
94	F	40.353	102.33	306.81
95	P	55.822	100.84	302.43
96	P	52.155	96.402	319.43
97	P	53.921	105.91	265.18
98	P	53.131	82.746	307.85
99	P	55.828	85.048	270.77
100	P	61.086	91.369	300.56

TRIALS: 100 YIELD: 60
(PASSED: 60 FAILED 40)

Mode YIELDP Results:

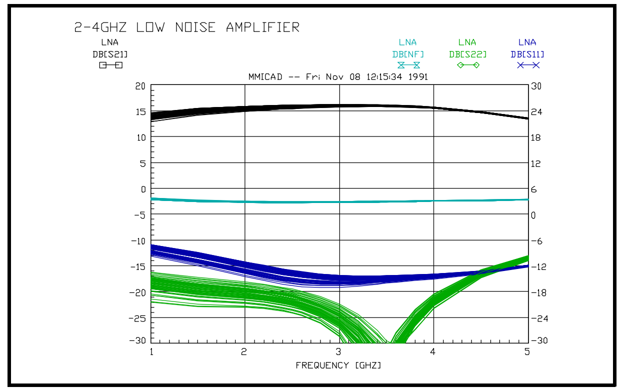

Figure 2 YIELDP Circuit Responses

MMICAD Yield Analysis

TRIAL		RSQ1	RSQ2	CSQ
53	P	49.490	104.42	313.56
54	P	46.819	95.194	326.45
55	P	55.756	90.557	308.30
56	P	55.836	94.406	306.20
58	P	50.731	85.517	310.12
61	P	47.775	98.074	299.13
62	P	50.355	89.110	284.05
64	P	50.917	107.64	269.26
65	P	41.229	94.252	269.79
69	P	46.961	101.09	281.10
71	P	47.470	87.699	302.37
73	P	54.339	94.300	295.90
74	P	53.642	101.42	316.35
76	P	47.119	89.241	297.20
77	P	53.006	90.167	273.57
79	P	60.697	91.602	315.58
80	P	43.739	102.54	313.22
81	P	56.677	84.732	333.91
82	P	50.264	99.463	298.75
83	P	49.277	98.545	264.66
84	P	59.777	94.805	313.13
86	P	53.883	108.48	263.92
89	P	53.322	100.65	292.10
92	P	50.370	99.228	296.04
94	P	41.147	91.853	321.33
95	P	46.939	100.55	311.97
97	P	54.082	101.46	292.09
98	P	51.343	87.000	294.60
99	P	48.242	85.837	318.15

TRIALS: 100 YIELD: 61
(PASSED: 61 FAILED 39)

TRIAL		RSQ1	RSQ2	CSQ
2	P	52.611	104.82	281.70
3	P	48.805	102.53	307.04
4	P	56.893	95.286	323.70
6	P	53.838	89.427	302.91
7	P	52.035	109.96	277.23
8	P	52.697	107.53	265.80
12	P	48.274	98.935	317.68
15	P	42.246	99.950	295.47
17	P	53.729	90.657	330.55
18	P	54.778	104.75	275.13
19	P	44.082	99.316	326.46
21	P	55.269	96.516	315.07
22	P	49.121	95.043	312.09
23	P	43.650	102.47	288.52
26	P	47.168	92.635	290.69
27	P	45.572	94.914	267.54
28	P	54.454	104.09	267.19
29	P	51.983	83.434	312.24
30	P	45.465	98.158	319.61
31	P	47.305	105.15	297.40
32	P	51.272	86.102	267.50
33	P	49.977	98.013	288.22
35	P	53.876	101.09	302.83
36	P	54.718	100.50	298.90
39	P	59.004	94.102	292.21
42	P	48.224	94.892	269.76
43	P	52.969	93.706	300.63
44	P	45.613	99.420	349.04
47	P	46.748	102.33	300.98
49	P	48.943	84.161	280.77
50	P	47.787	102.30	307.39
51	P	52.231	97.434	296.44

Yield Analysis Example

To assess the influence of varying the technological sheet resistance parameters, a Monte Carlo simulation run of 100 trials will be performed. It should be noted that the number of trials would normally exceed 500 to ensure that the results are statistically relevant.

Circuit file:

```
FILE NAME:      LNA2.CKT
NOTES:          A low noise 2-4 GHz amplifier design based on MMICs.
                Monte Carlo Analysis.
                Vary the technological sheet resistance parameters over a
                normal distribution.  (See the VAR block below.)

MODE YIELD

GLOBAL
  DIM  FREQ=1e+009  RES=1  COND=0.001  CAP=1e-012  IND=1e-009
LNG=1e-006 TIME=1e-012
 MSUB ER=12.8 H=200 T=3 RHO=1.3 TAND=0 @SUB0

FILES
 C:\EXAMPLES\F3002.S2P F3002 101 2P FREQ

VAR
 LRFB=  92.1344
 NIN1=  2.5063
 LOUT1= 127.864
 NIN2=  1.53149
 NOUT2= 3.481
 RSQ1= $ 50 5 $
 RSQ2= $ 100 10 $
 CSQ=  $ 300 20 $
CKT
 !Square Spiral Inductor Model with N=Number of Turns as Parameter:
 MODVAR N=3.00739
 SRL 1 2 R={ .233*N + .0927*N*N } L={ -.164*N + .286*N*N }
 CAP 1 2 C={ .002*N - 6E-5*N*N }
 CAP 1 0 C={ .0175*N+ 1.15E-4*N*N }
 CAP 2 0 C={ .0121*N+ 1.86E-4*N*N }
 DEF2P 1 2 SPIR ( N  )

 !Distributed Thin Film Resistor Model with W, L, and RSQ as Parameters:
 MODVAR W=20 L=91.4649 RSQ=100
 RES 1 2 R={ RSQ*L/W }
 MTRLND 2 3 W={ W } L={ L } @SUB0
 DEF2P 1 3 TFRES ( W L RSQ  )

 !Drain Bias Network for Stage#1 and Stage#2:
 TFRES 1 2 0 W=20 L=40 RSQ=RSQ1
 SPIR 2 3 0 N=3.5
 SLC 3 0 L=0.1 C=1000
 DEF1P 1 DBIAS

 !Stage#1 of the Amplifier:
 SRC 1 0 R=5000 C=10
 SPIR 1 2 0 N=NIN1
 F3002 2 3 10 M=4
 MTRL 10 11 W=20 L=400 @SUB0
 RES 11 0 R=25
 CAP 11 0 C=20
 MTRL 3 4 W=12 L=LOUT1 @SUB0
 TFRES 2 20 0 W=20 L=LRFB RSQ=RSQ2
 TFC 4 20 W=225 L=200 CS=CSQ @SUB0
 DBIAS 4 0 M=1
 DEF2P 1 4 STAGE1

 !Stage#2 of the Amplifier:
 MTRL 1 2 W=12 L=250 @SUB0
 SRC 2 0 R=5000 C=4
 SPIR 2 3 0 N=NIN2
 F3002 3 4 10 M=2
 MTRL 10 11 W=100 L=50 @SUB0
 RES 11 0 R=50
 CAP 11 0 C=20
 SPIR 4 5 0 N=NOUT2
 DBIAS 5 0 M=1
 DEF2P 1 5 STAGE2

 !Final Amplifier Construction:
 STAGE1 1 2 0 M=1
 TFC 2 3 W=200 L=135 CS=CSQ @SUB0
 STAGE2 3 4 0 M=1
 DEF2P 1 4 LNA

PARAM
SWEEP 1 100 1

MARKER
 STEP 1 1.5 2 2.5 3 3.5 4 4.5 5

FREQ
 STEP   1 1.5
 SWEEP  2 4 0.2
 STEP   4.5 5
OPT
 RANGE 2.0 4.0
 LNA DB[S21] IN 15.5 0.7  W=100
 LNA DB[S22] LT -15  W=50
 LNA DB[S11] LT -11  W=50
 LNA DB[NF] LT 3.2  W=100

OUT
 LNA DB[S21] AMP
 LNA DB[S11] AMP R
 LNA DB[S22] AMP R
 LNA DB[NF] AMP R
 LNA VSWR[S11] VSWR
 LNA VSWR[S22] VSWR
 LNA RE[K] k
 LNA DB[NF] NFIG
 LNA  GPCIR 1 GPCIRC
 LNA  SMI[GM2] GPCIRC
 LNA  NCIR 1 NCIRC
 LNA GOPT NCIRC
 LNA AMP STAB
 LNA SPAR LNA_SPAR
 F3002 SPAR FET_SPAR

GRID
 RANGE 1 5 1
 AMP -30 20 1 R -30 30
 ERRFCT 50 250 0 10
 VSWR 1 5 0 4
 NFIG 1 5 0 4
 k 1 5  0 40

LABEL
2-4GHZ LOW NOISE AMPLIFIER
```

Mode YIELDF Results:

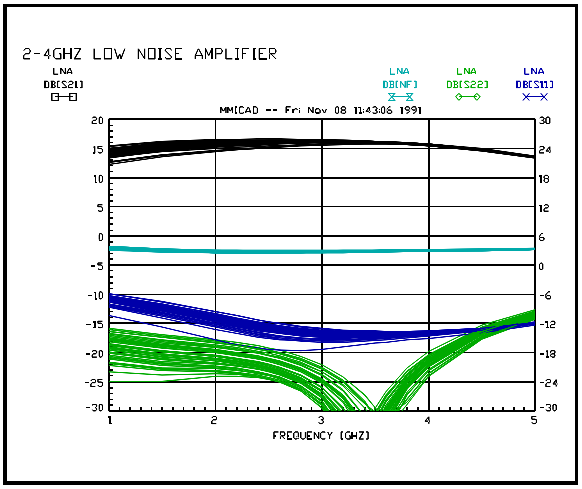

Figure 3 YIELDF Circuit Responses

MMICAD Yield Analysis

TRIAL		RSQ1	RSQ2	CSQ
1	F	48.162	116.90	297.51
3	F	49.328	112.16	314.64
4	F	48.784	105.06	330.55
5	F	49.902	113.17	306.26
9	F	56.280	114.48	309.89
10	F	53.257	108.40	317.52
17	F	46.649	114.80	279.54
20	F	46.380	106.17	305.78
23	F	43.754	108.51	298.32
27	F	57.993	104.68	302.21
28	F	52.299	105.72	328.51
32	F	49.358	109.12	330.82
34	F	41.609	86.353	298.99
35	F	47.263	120.18	314.24
36	F	41.490	119.94	308.12
37	F	51.298	106.13	322.51
38	F	53.863	120.92	315.07
40	F	54.000	109.46	303.38
41	F	41.243	102.62	303.63
42	F	47.855	112.37	317.31
47	F	52.783	111.14	340.93
48	F	39.303	90.299	268.17
49	F	52.733	110.84	292.76
51	F	43.303	106.09	310.27
57	F	45.117	110.66	309.69
58	F	49.558	131.03	309.55
60	F	62.679	113.92	271.10
61	F	47.607	109.35	290.49
65	F	52.171	118.84	287.72
68	F	36.959	86.515	328.41
69	F	63.568	101.88	301.59
70	F	54.624	77.974	310.57
75	F	40.908	110.44	286.49
77	F	60.483	101.40	273.58
79	F	47.386	107.83	312.34
81	F	57.591	126.37	306.63
83	F	44.317	83.151	262.87
86	F	42.899	110.40	281.60
90	F	45.795	112.60	284.18
91	F	43.285	104.53	293.62
97	F	60.290	104.98	286.31
100	F	45.752	108.30	251.48

TRIALS: 100 YIELD: 58
(PASSED: 58 FAILED 42)

After analysis, the designer is provided a list of correlated circuit variables that resulted in either a pass or fail condition.

Of course, this tabular data response may be saved to disk, allowing the designer to perform a post processing statistical analysis. The following plots were created using GRAPHER™ with the YIELD tabular data as input:

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