

Using MMICAD to Design Lumped Element Diplexers

by Kevin G. Faisyn

MMICAD's new filter synthesis module, FAISYN™, enables RF and microwave design engineers to quickly synthesize and simulate lumped element filters, diplexers and multiplexers.

This article shows how FAISYN can be used to help design a lumped element diplexer for a typical receive subsystem application. The discussion includes the function of the diplexer in the receive system, an overview of the design procedure, and the results of the MMICAD simulation.

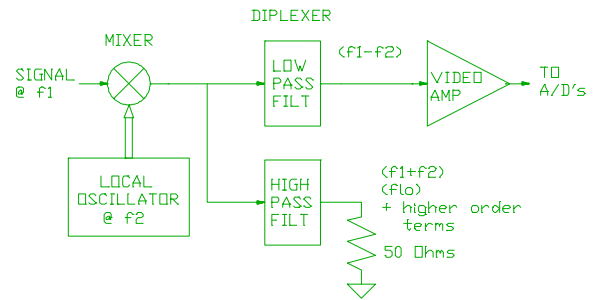
Diplexers Improve Receiver Performance

An important figure of merit in receiver design is the two tone output third order intercept point (OTOI). The OTOI is one of the key parameters used in determining receiver dynamic range. Mixers are major contributors to OTOI degradation in receivers. It has been shown that the intermodulation performance of mixers can be improved if care is taken to properly terminate undesired leakage signals and mixing products. One way to do this is through the use of diplexing filters.

A diplexer is basically a frequency multiplexer that splits a single channel carrying many frequencies into two channels carrying fewer frequencies. In the design presented here, frequency selectivity is accomplished by placing a low pass filter in parallel with a high pass filter.

The block diagram in Figure 1 shows the receiving subsystem under consideration. The diplexer sees a 50 ohm impedance looking into the amplifier and back at the mixer. The IF signal to the mixer is at 150 MHz, with signal bandwidth of 40 MHz. The mixer LO frequency is at 150 MHz. The mixer output consists of an information occurring at frequencies below 20 MHz, an undesired signal at the sum frequency, 300 MHz, and LO leakage at 150 MHz.

All of these signals enter the diplexer where they are split. The desired signal is passed through the low pass channel to the amplifier.



$f_1=150\text{ MHz}, f_2=150\text{ MHz}$

Figure 1 Typical receive subsystem. The diplexer is formed by paralleling singly terminated low and high pass filters derived from the same normalized low pass prototype.

The undesired signals are passed through the high pass channel and are dissipated in the 50 ohm resistor. Terminating the undesired signals in this manner minimizes reflections back into the mixer where further harmonic generation can occur.

Design Procedure

The diplexer is designed using the procedure outlined in *Microwave Filters, Impedance Matching Networks, and Coupling Structures* by Matthai, Young and Jones. The approach is to base the design on the singly terminated normalized low pass filter of Figure 2.

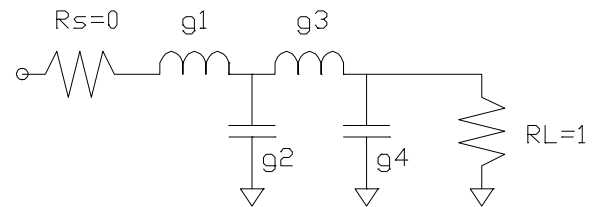


Figure 2 Singly terminated, normalized low pass filter.

Once a suitable filter type is selected, frequency and impedance transforms are used to derive the low and high pass filters. These derived filters have the same 3 dB frequency and are said to be complimentary filters.

When designed using the above method, the susceptances of the individual filters will nearly cancel when they are connected to form the diplexer. This results in an input impedance which is nearly constant at 50 ohms over a broad frequency range.

Circuit Specification

A typical diplexer specification is as follows,

- System impedance = 50 ohms**
- Passband response = 0.01 dB Chebyshev**
- 3 dB cross over frequency = 50 MHz**
- Rejection at LO frequency = 40 dB min.**
- Input S11 = -10 dB max.**
- Number of poles, N = 4**

A couple of comments are in order concerning these specifications. First, the 3 dB frequency is two and one-half times the signal band width. While this may seem excessive, it should be remembered that second harmonic generation will be low if a good double-balanced mixer is used and the wider band width ensures good phase linearity for the signal, an important consideration in pulse systems.

Finally, the number of poles required, N=4, has been estimated from the rejection requirement and the knowledge that low pass filters roll off with a 6*N dB/Octave slope once past the 3 dB frequency. Thus our filter skirt should be approximately 24+3=27 dB down at 100 MHz and 48+3=51 dB down at 200 MHz, enough to meet our requirement with some design margin.

Diplexer Synthesis using FAISYN

The diplexer is designed using singly terminated low and high pass filter sections with a 0.01 ohm source impedance and a 50 ohm load. The networks synthesized by FAISYN are shown in Figure 3, the MMICAD circuit files written by FAISYN for the low and high pass sections have been combined into the listing in Figure 4. The results of the MMICAD simulation (shown in Figures 5-7) clearly shows that all of the design goals have been met.

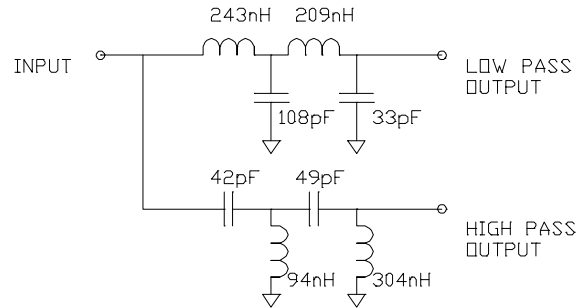


Figure 3 The diplexer network as synthesized by FAISYN

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===== FILTER SYNTHESIS PROGRAM V1.0 =====
!
! Chebyshev DIPLEXING Filter
! N= 4
! 3 dB frequency= 50.0000*1E6
! FILENAME= DIPLEX.CKT
!
!===== (c) 1992: OPTOTEK / K.FAISON =====

GLOBAL
DIM  FREQ=1E6 CAP=1E-12 IND=1E-9

CKT
IND 1 2 L= 243.3010
CAP 2 0 C= 107.8402
IND 2 3 L= 208.8466
CAP 3 0 C= 33.2882
DEF2P 1 3 LPfilter

CAP 1 2 C= 41.6444
IND 2 0 L= 93.9550
CAP 2 3 C= 48.5147
IND 3 0 L= 304.3757
DEF2P 1 3 HPfilter

! Form diplexer by parallelling LP and HP filters

LPfilter 1 2
HPfilter 1 3
DEF3P 1 2 3 DIPLEXER

FREQ
SWEEP 5.0000 400.0000 2000

OUT
DIPLEXER DB[S21] TRANS1
DIPLEXER DB[S31] TRANS1
DIPLEXER DB[S11] TRANS1 R
DIPLEXER DB[S21] TRANS2
DIPLEXER DB[S11] TRANS2 R
DIPLEXER S11 SMITH
DIPLEXER SPAR SPAR

GRID
RANGE 0.0000 150.0000 25.0000
TRANS1 -50 0 10 R -50 0
RANGE 5.0000 50.0000 9.0000
TRANS2 -5 0 0.5 R -60 0

LABEL

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Figure 4 The MMICAD Circuit File

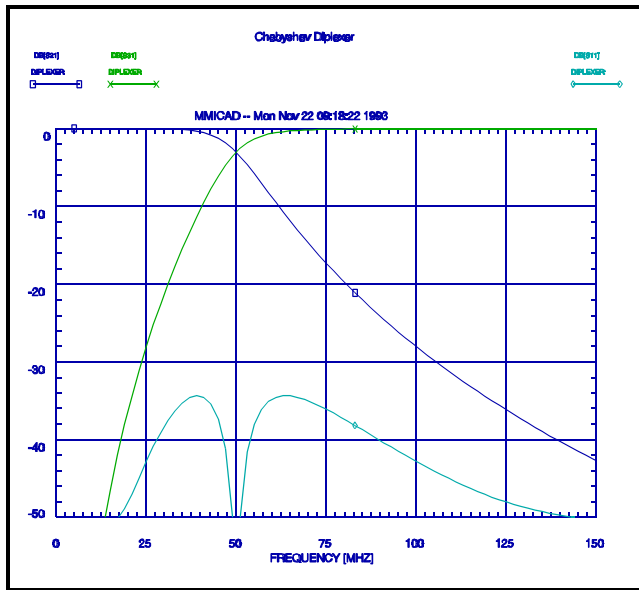


Figure 5

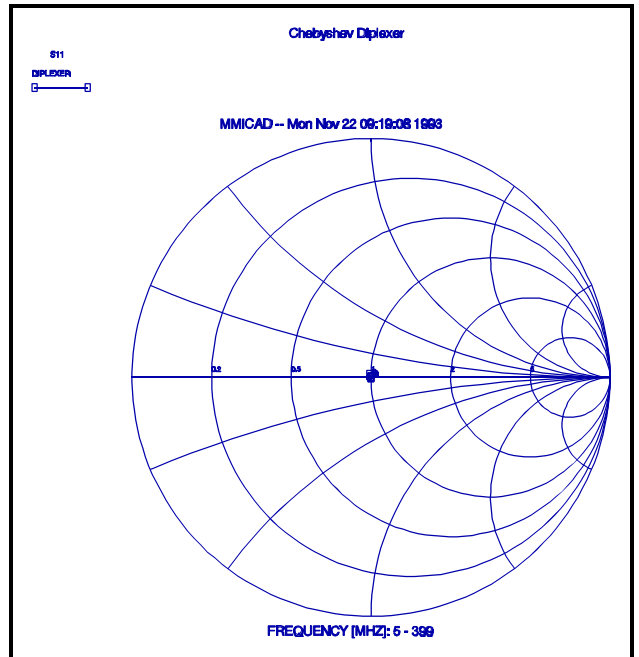


Figure 7

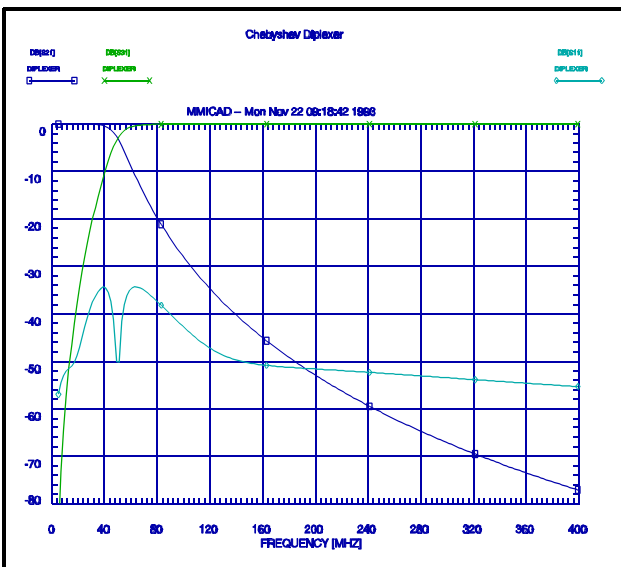


Figure 6