

Yield Forecasting of Active Microwave Devices

FETPro and MMICAD

FETPro™ is a physics-based MESFET simulator from GaAsCode. It allows the microwave performance of MESFETs to be forecast from the device physical structure (including the metallurgical gate length, channel doping profile, gate recess depth, surface potential and so on) and the bias applied to the FET.

Using FETPro in conjunction with **MMICAD™** allows circuit designers to perform true, physics-based, sensitivity analysis and Monte Carlo yield analysis of circuits incorporating FETs.

The underlying basis of, and need for, technology-level simulation of MICs and MMICs incorporating FETs is discussed in MMICAD Application Note 28.

Examples

The following figures are sample screen displays taken from combined FETPro/MMICAD simulations of a two-stage, reactively matched, 44GHz satellite communications amplifier. The amplifier is designed to provide a gain of greater than 12.5dB from 42 to 46GHz, with S_{21} and S_{22} matches better than -12dB and -15dB, respectively.

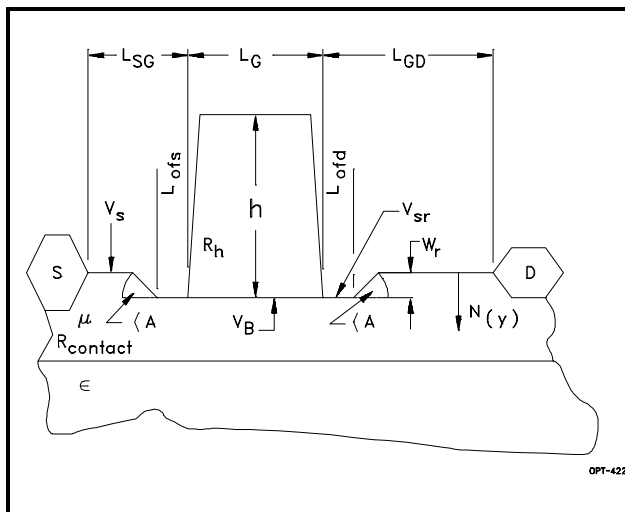


Figure 1

In each example, the microwave behaviour of the FETs is calculated by FETPro, which is invoked from the Links menu in MMICAD. FETPro automatically writes data files for MMICAD and also automatically edits the circuit description (netlist) for MMICAD to use in the overall circuit simulations. The details of this procedure are given at the end of this note.

The sensitivity analyses show rather extreme changes in circuit performance, which are characteristic of the high frequency of operation and the circuit topology used. At lower frequencies these effects are usually smaller, but the principle is unchanged.

Figure 1 shows several of the structural dimensions and material parameters specified in FETPro. The bias applied to the device is also specified. The measured profile used in these examples is shown in Figure 2. Figure 3 is the circuit schematic of the amplifier.

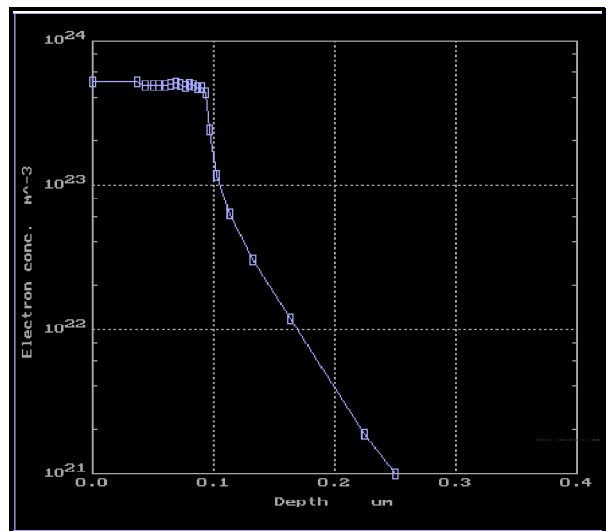


Figure 2

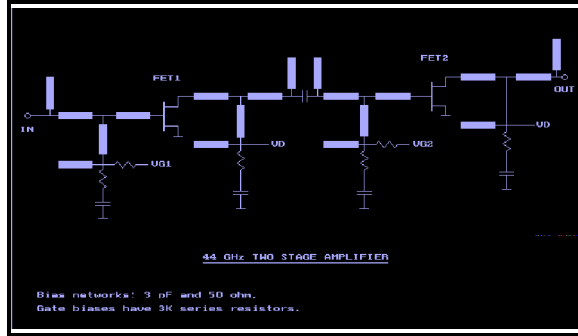


Figure 3

Figure 4 shows an example of a circuit sensitivity analysis: what happens if the FETs' drain bias decreases from the nominal value of 2.0V as the power supply drifts over time? (Such issues are crucial in space-borne applications.) The circuit response is shown (S_{21} , S_{11} and S_{22}) for drain biases between 1.5V and 2.0V, in steps of 0.1V. The values for S_{21} are read off the left-hand vertical axis; the matches are plotted using the right-hand vertical scale. The largest forward gain occurs for the 2.0V drain bias, the design response. Return losses improve with decreasing drain bias over the majority of the frequency range. From the curves, it is evident that the amplifier fails to meet the forward gain specification for drain biases less than 1.8V.

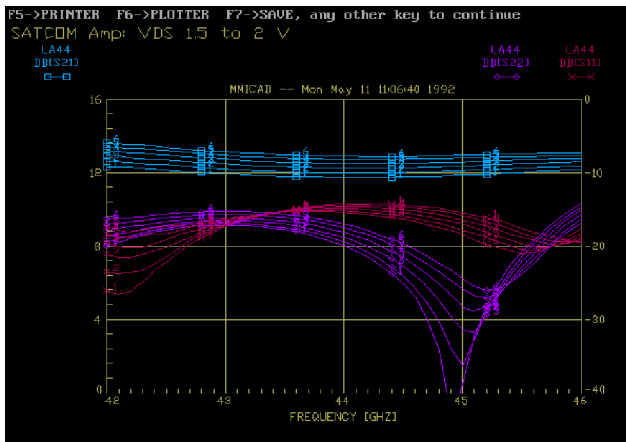


Figure 4

Figure 5 shows a further example of sensitivity analysis, which answers the question "what happens if the gate length varies from its nominal value of 0.20 μ m?". The graph shows the effect on overall circuit S_{21} and S_{22} of changing the gate length from 0.17 to 0.23 μ m, in 0.01 μ m steps. As might be expected, the forward gain of the amplifier decreases with increasing gate length. Examination of the curves shows that only the gate lengths of 0.19 μ m and 0.20 μ m meet all three circuit specifications.

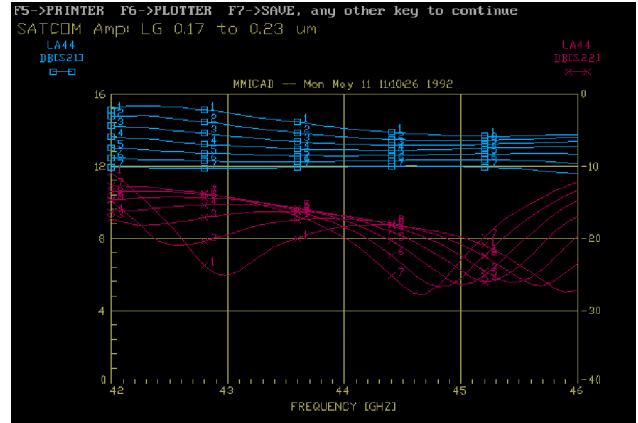


Figure 5

Of course, for most circuit designers, the option of changing a standard device gate length does not exist. However, for "first pass" design success, the effect of the inevitable variations in fabricated gate lengths (and other physical parameters) on the overall circuit response should be considered before committing a design to fabrication.

In general, no one technological parameter varies alone; there are spreads in every parameter. Figure 6 shows the density plot result of a Monte Carlo yield analysis. Each curve is a possible amplifier response, resulting from placing different simulated FETs into the amplifier circuit. For every FET simulation, a value is randomly chosen (from within a Gaussian distribution around the nominal value) for each physical parameter affecting the FET. Each combination of parameters represents a possible physical outcome of FET fabrication. The microwave performance of each FET, simulated by FETPro, is substituted in the overall MMICAD simulation. Figure 7 provides an overview of the Monte Carlo analysis procedure.

In Figure 6, 100 circuit responses, corresponding to 100 different FETs, are shown. In addition to simulating 100 different FETs, variations in the four 50 Ω bias resistors were simulated by specifying a Gaussian distribution of values around the nominal value. As indicated under the graph, 43 percent of the circuits are predicted to meet the circuit specifications. (For a statistically meaningful yield forecast, around 500 simulations would be required; Figure 6 serves only as an illustration of a density plot.)

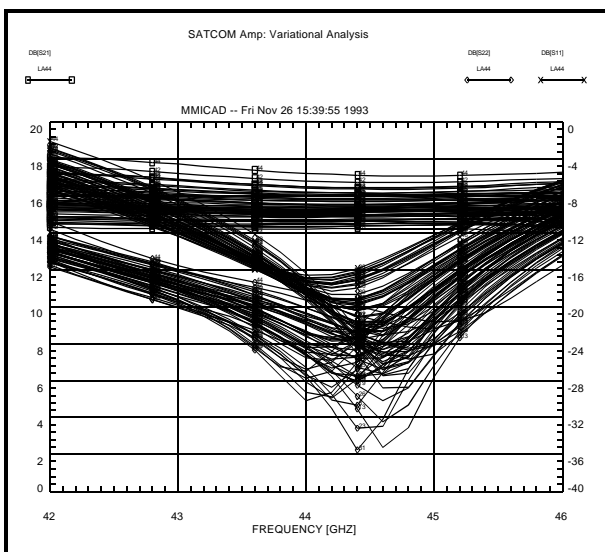


Figure 6

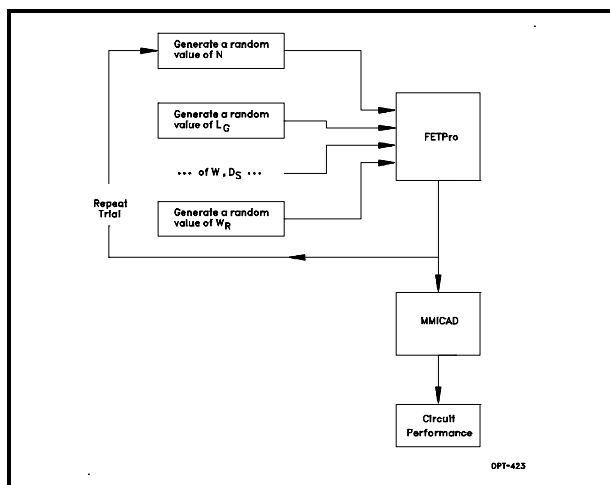


Figure 7

Data Transfer Between FETPro and MMICAD

FETPro and MMICAD are designed to work as interactive, stand-alone programs or together for technology-level simulation of FETs and circuits. The interface between the programs is designed so that data can be automatically passed between the programs with minimal intervention from the user and so that the programs appear fully integrated.

The information presented here illustrates the use of several of the unique features of MMICAD.

FETPro can be invoked from the Links menu in MMICAD. The microwave performance of each FET simulated in FETPro is stored in a data file for subsequent use by MMICAD. In addition to performing the FET simulations, FETPro also automatically edits the MMICAD netlist of the

circuit to pass the data to MMICAD. Figure 8 shows several parts of the netlist modified by FETPro for the Monte Carlo simulation example.

FETPro assigns sequential filenames to the files created for each simulated FET. The names have a three-letter prefix, followed by the number of the FET trial simulation; for example AAA1.SIM, AAA2.SIM and so on.

FETPro edits the FILES block and the PARAM block in the netlist so that MMICAD will use the 100 FET files generated. During the Monte Carlo analysis, the ? in the files block is replaced by the number of the current trial so that each FET file is read in turn. The capability of reading multiple data files during a single overall yield analysis is a feature not found in microwave simulators other than MMICAD.

The LABEL block is also modified by FETPro to indicate what simulation has been performed. A modified label appears above each of the graphs (Figures 4, 5 and 6).

The new netlist written by FETPro is given the three-letter prefix as the filename, for example, AAA.CKT. The simulation in MMICAD is invoked by selecting Variational Analysis from the Run menu, after loading the new circuit file using the Files menu.

The four 50Ω bias resistors are set equal to variable RBIAS in the CKT block of the file. In the VAR block, the assignment

$$RBIAS = \$ 50 \ 3 \ \$$$

results in a value for RBIAS being selected for each trial from within a Gaussian distribution which has a mean of 50Ω and standard deviation of 3Ω.

The combination of the MODE YIELD and the OPT specification causes each simulated amplifier response to be compared with the specification to determine whether the trial passes or fails.

The syntax of the MODE, OPT and VAR blocks for Monte Carlo yield analysis is discussed further in MMICAD Application Note 5.

FETPro is a trademark of GaAsCode Ltd., Cambridge, England. MMICAD is a trademark of Optotek Ltd., Kanata, Canada.

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MODE YIELD

FILES
D:\MMICAD\WORKING\aaa?.SIM GCF 101 2P FREQ

VAR
RBIAS= $ 50 3 $
.
.

! Circuit description:

CKT
.
.
RES 4 5 R=RBIAS
CAP 5 0 C=3
.
.

FREQ
SWEEP 42 46 .1

PARAM
SWEEP 1 100 1

OPT
LA44 DB[S21] GT 12.5 W=1
LA44 DB[S11] LT -12 W=1
LA44 DB[S22] LT -15 W=1

OUT
LA44 DB[S21] ALL

GRID
ALL 42 46 0 16 R -40 0

LABEL
SATCOM Amp: 100 Monte Carlo trials
```

Figure 8