

# Technology-Level Simulation of Active Microwave Circuits

## FETPro and MMICAD

**FETPro™** is a physics-based MESFET simulator from GaAsCode. It allows the microwave performance of MESFETs to be forecast from the device physical structure (including the metallurgical gate length, channel doping profile, gate recess depth, surface potential and so on) and the bias applied to the FET.

Using FETPro in conjunction with **MMICAD™** allows circuit designers to perform true, physics-based, sensitivity analysis and Monte Carlo yield analysis of circuits incorporating FETs.

## Circuit Design

Circuit designers can use the FETPro/MMICAD software solution to answer questions such as:

- (i) *"For a given FET structure, what bias condition will best satisfy the circuit specification?"*
- (ii) *"How will my circuit response change if the bias supply drifts over time?"*
- (iii) *"How sensitive is my circuit to unavoidable spreads in technological parameters: for example, will the circuit still meet the specification if lithography errors result in FETs with a gate length of  $0.55\mu\text{m}$  instead of  $0.5\mu\text{m}$ ?"*
- (iv) *"What is my true circuit yield, taking inter-element correlations into account?"*
- (v) *"Can my hybrid circuit yield be improved by pre-selecting discrete FETs with a particular range of pinch-off voltages?"*
- (vi) *"Can my MMIC yield be increased by reducing the processing tolerance on the gate recess depth (or any other given technological parameter)?"*

- (vii) *"Can my MIC or MMIC yield be improved simply by changing the method used to bias the FETs?"*

## Why is Technology-Level Simulation Important?

FET-based MICs and MMICs are usually designed around a nominal FET, which is intended to be characteristic of the foundry process (for MMICs) or the manufacturer's discrete devices (for MICs). Inevitably, the measured responses of most of the fabricated circuits are different from the simulated response.

Deviations from the design response arise from unavoidable spreads in the technology used to fabricate the FETs and other circuit components. If these spreads are not correctly included in simulations during the design phase, the yield of fabricated circuits which "meet the specification" may be unacceptably low and commercially non-viable.

In many circuit designs, the measured deviations of the overall circuit response are dominated by variations in the microwave performance of the FETs in the circuit. One reason for this dominance is simply that the passive elements (such as transmission lines) are considerably larger than the FETs, so that any tolerances in lithography, for example, have a greater influence on the FET performance.

A deviation from the nominal value of any given physical parameter (for example, the gate recess depth in a fabricated FET may be  $0.05\mu\text{m}$  instead of the intended value of  $0.045\mu\text{m}$ ) does not result in a change in only one FET equivalent circuit element. Almost all the equivalent circuit elements will be different from their nominal values. In addition, the changes in the equivalent circuit elements are correlated with each other.

Consequently, the effects of technology spreads on overall circuit performance cannot be forecast by simply varying the values of FET equivalent circuit elements one at a time, nor by varying all equivalent circuit elements simultaneously, without regard for the correlations between them [1].

By varying the actual technological parameters in the circuit analysis, the changes in all equivalent circuit elements are correctly simulated and the correlations between the elements are inherent in the calculation.

### Monte Carlo Yield Analysis and Sensitivity Analysis

The overall procedure for Monte Carlo analysis is shown in Figure 1.

In circuit fabrication, all technological parameters have spreads around their nominal values. For every FET simulation in a Monte Carlo analysis, a value is randomly chosen (from within a specified distribution around the nominal value) for each physical parameter affecting the FET. Each combination of parameters represents a possible physical outcome of FET fabrication. The microwave performance of each FET is simulated by FETPro and the results saved for use by MMICAD. This procedure is repeated for each trial required in the overall Monte Carlo analysis.

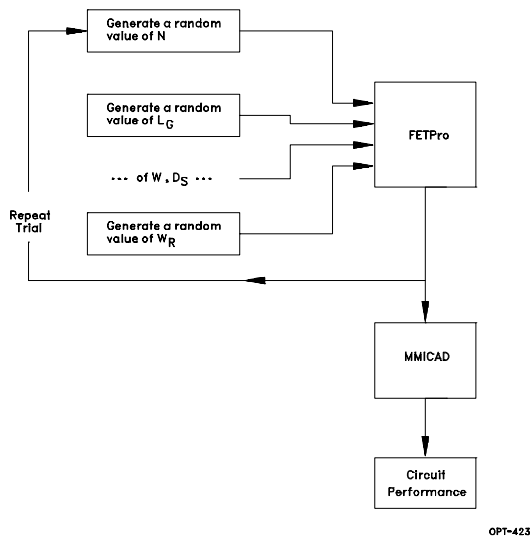


Figure 1

MMICAD then substitutes each simulated FET in the circuit in turn and calculates the full circuit response. As part of this process, random variations in any of the passive circuit elements are also included in the simulation [2].

Figure 2 shows a typical density plot resulting from a Monte Carlo analysis. Each curve is a physically-possible amplifier response. The yield of working circuits is forecast by comparing each simulated circuit response with the design response.

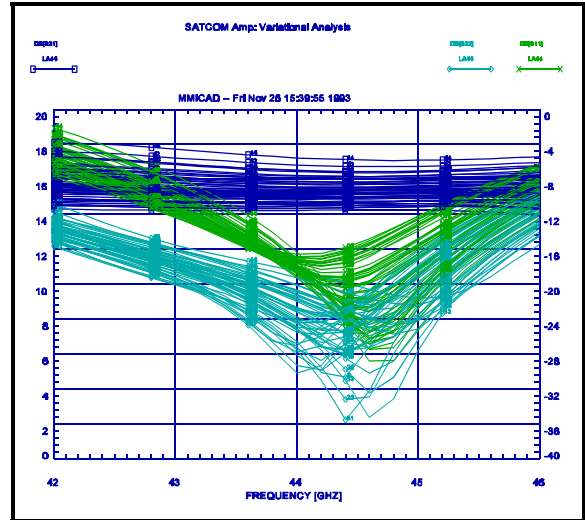


Figure 2

Sensitivity analysis differs from Monte Carlo analysis in that only one technological parameter, or applied bias, is varied to investigate its effect on the full circuit response. In addition, the variation is systematic rather than random. Examples of FETPro/MMICAD technology-level sensitivity analyses and Monte Carlo analysis of circuits are given in MMICAD Application Note 29 [3].

### The FETPro/MMICAD Interface

FETPro and MMICAD are designed to work as stand-alone programs or together for technology-level simulation of FETs and circuits. The interface between the programs is structured so that the programs appear fully integrated and that data can be automatically passed between the programs with minimal intervention by the user.

The fast execution speed of both programs means that overall simulations are executed very rapidly. The Monte Carlo analysis result shown in Figure 2, requiring the simulation of 100 FETs and 100 circuit responses, was executed in less than 3 minutes on a 33MHz 486 PC with a 2MB RAM disk. The circuit has 33 components and was simulated at 40 frequency points per circuit analysis [2].

FETPro can be invoked from the **Links** menu in MMICAD. The programs can be used together for simulations without requiring any additional computer resources beyond the 640K memory of standard personal computers. If additional memory is available and the computer is correctly configured for a RAM drive [3], then the overall simulation time will be reduced. Details of the interface are given in MMICAD Application Note 11.

## Are There Viable Alternatives to Technology-level Simulation?

When a single MIC circuit is required to be built around a single sample FET, then the best circuit design approach is to measure the FET at dc (I-V measurements) and RF (S-parameter and noise parameter measurements) for each bias point required and to use this data directly in the circuit design. However, when more than just a few circuit samples are needed, a new circuit cannot be designed for each device and this method cannot be used.

The Monte Carlo yield analysis scheme outlined above is physically realistic because the correlations which exist between FET equivalent circuit elements are automatically present in the simulation. The correlations all have a common origin -deviations in the physical FET structure.

Approaches other than technology-level simulation all involve assembling a large database of measured FET data, which is intended to be representative of the device being used. While there are differences in how the measured data is processed and stored, the underlying measurement process is fundamental to these approaches.

To fully characterise a single FET type in a given single process may require measuring dc data as well as S-parameter and noise data from around 500 sample FETs (to ensure statistically meaningful results). For each FET, measurements at around 40 bias points would be required, with around 20 frequency points required per bias point. (Such a level of effort is seldom expended in practice.) Accurate Monte Carlo analyses could then be made by substituting each measured FET (at the required bias point) in turn into the circuit netlist and simulating the circuit response. Since actual measurements are used there are no correlations to be kept.

Clearly though, the amount of data storage required prohibits such a direct approach. Several data reduction and interpolation schemes have been developed, for example EEsos's Truth Model™ and Shadow Model™ [4]. If these methods successfully retain all the required 66 correlations between equivalent circuit elements, then accurate results are possible.

There are, however, fundamental weaknesses in the database approach. Most important of these is that the database is extremely difficult to maintain. Each time a process shifts (whether intentionally or not), the entire device characterisation procedure must be repeated. If there are different FET variants on the same fabrication line, then each FET must be re-characterized. By contrast, in technology-level simulation, changes in the fabrication process require only simple changes to the input to the FET simulator. (Indeed, the underlying

causes of unintentional process shifts over time can often be traced by simulating the effects of changes.) These changes are immediately applicable to all FET variants produced in the process.

Second, assume that a yield analysis produces a predicted yield which is too low for commercial viability. If the analysis is founded on the database approach, then the circuit designer can do nothing but accept the result. On the other hand, with technology-level analysis, the designer can identify which technological tolerances are responsible for the low yield. An example of this approach is given in reference 5.

Design centering using the database approach must always treat the FET as a fixed element which cannot be centred. This is a severe limitation given that the FET performance often dominates the circuit performance. A circuit specification which is impossible to meet with a fixed FET may well be achievable with only minor changes to the FET: only technology-level simulation allows this possibility to be investigated [5].

Other weaknesses of the database approach, such as the inability to trouble-shoot circuits which do not meet the specification, apply but are beyond the scope of this application note.

Some examples of technology-based simulation of circuits using FETPro/MMICAD are given in MMICAD Application Note 29.

- [1] Application Notes GC-AN10 and GC-AN13, GaAsCode Ltd., 1991.
- [2] MMICAD Application Note 5, Optotek Ltd., 1992.
- [3] MMICAD Application Note 11, Optotek Ltd., 1992.
- [4] jOmega Product Literature, EEsos Inc., 1991.
- [5] Ladbrooke P.H., Hill A.J. and Bridge J.P., "CAD for GaAs MMIC Manufacture-ability", 1990 GaAs IC Symposium Digest, pp. 335-338.

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