Computer Aided Design of MMIC Variable Attenuators

Introduction

Variable attenuators have been widely used in telecommunications and electronic warfare applications to adjust the signal level or to compensate for intrinsic gain variations with operating temperature. This application note details the design, fabrication and testing of a high performance, 3-7 GHz, voltage controlled MMIC attenuator which was designed using MMICAD™, Optotek's linear analysis and design software.

Background

GaAs MESFETs at zero drain bias have been used as variable resistors to construct a 'T'-type attenuator [1,2,3]. The impedance matching condition and attenuation as a function of the resistance values for the series and shunt MESFET are presented in Figure 1. This idealized model does not take into account the series and parallel parasitic capacitances which are present in real MESFETs.

To properly account for the influence of these parasitics, a bias-dependent common-gate, zero-drain-bias model for the Optotek cell library of MESFETs, was developed [4]. This model was developed by using MMICAD™ to control a Wiltron 360 Automatic Network Analyzer in combination with a Design Technique Probing Station to extract the S-parameters of the MESFETs under bias. MMICAD allows for the optimization in real time to an equivalent circuit model. By using this software to control a DC programmable power supply source, the bias on the MESFET is automatically ramped while the optimization results are extracted and stored in files. Finally, the tabular data of each element in the model as a function of bias is fitted numerically with pinchoff voltage function as the variable. The model used is shown in Figure 2 along with the element values for a 600 micron MESFET. A distributed RC line has been used to simulate the characteristic of the channel region of the device, including voltage dependent values for the distributed resistance and capacitance. Lumped elements are included to take into account the parasitics of the extrinsic MESFET; these elements are not bias point dependent.

Example

To illustrate this technique, S-parameter measurements for a drain voltage of Vd=0V were performed on a 600µm wide device for gate voltage Vg ranging from 0 to 1.1 times the pinchoff voltage Vp. The measured S-parameters have been used to determine the extrinsic element values and the variation of the voltage dependent values for the resistance and the capacitance of the distributed RC line.

The dependence of these parameters was fitted in order to obtain a polynomial expression as shown in Figure 3. Also illustrated in this figure is the MMICAD simulation file that incorporates this equivalent circuit as a user-defined model along with measured and simulated S parameters at 20% of pinchoff for an Optotek 600 micron transistor.

All MESFETs in the attenuator operate in the passive mode by controlling the MESFET's linear operating region with gate bias. For each circuit topology, two independent gate biases are used, one to control the series MESFETs, and one to control the shunt MESFETs. The circuits use MESFETs as variable resistors; their models, in the simplest approximation, are resistors and capacitors in parallel. R varies as a function of bias and MESFET width. C varies slowly with bias, but is a function of MESFET width. Using the MESFET nonlinear model, the performance of the T-attenuator was optimized as a function of gate length in the 3-7 GHz frequency range using MMICAD. The optimal configuration in terms of attenuation profile, insertion loss and matching was determined to have two series 600 micron transistors and one 600 micron shunt transistor.

On the basis of switching speed, resistor values in series with the gate were optimized to be 2000 ohms; 20 pF capacitors were chosen for coupling and bypass.

The final MMICAD optimized electrical schematic is shown in Figure 4, while Figure 5 presents the simulated insertion loss and matching, both as a function of bias.

MMIC Layout

The design was laid out using 0.5 micron design rules. The final chip layout is shown in Figure 6. The size of the chip is 1040 x 925 microns. The MMIC's were fabricated using Optotek's foundry facilities [5].

Testing

The performance of the attenuator was evaluated by mounting the circuits on a gold plated brass test jig with APC 3.5 connectors. S-parameter measurements as a function of bias were made on a Wiltron 360 Network Analyzer. The bias points were chosen to match the simulated flat attenuator profile shown in Figure 5. The results are presented in Figure 7 which match closely the simulated performance.

As deep channel, high current MESFETs are chosen from this design, power handling is not considered to be a problem.

Conclusion

For the T-type 3-7 GHz attenuator designed using MMICAD™ design software and processed using standard GaAs foundry components, simulated performance agreed very closely with measured data.

References

[1] Tajima, Y., Tsukii, T., Mozzi, R., Tong, E., Hares, L. and Wrona, B., "GaAs monolithic wideband (2-18 GHz) variable attenuators", 1982 IEEE MTT Symp. Dig., pp 479-481, IEEE, New York, 1982.

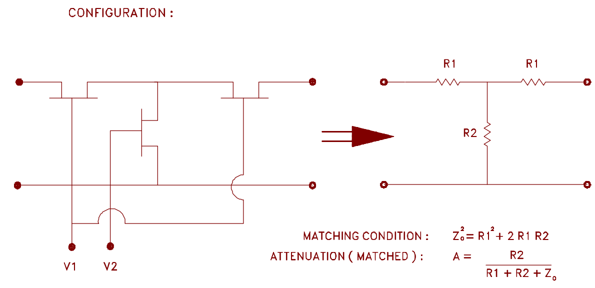
[2] Barta, G.S., Jones, K.E., Herrick, G.C. and Strid, E.W., "A 2 to 8 GHz leveling loop using a GaAs active splitter and attenuator", 1986 IEEE Microwave and Multimeter-wave Monolithic Circuits Symp., pp 75-79, IEEE, New York, 1986.

[3] Landry, P.P., Internal Report, Spar Aerospace Ltd., February 1987.

[4] Pucel, R., "Signal and noise properties of GaAs microwave MESFETs", Adv. Electron. Electron Phys., 38, 193-265, 1975.

[5] Dindo, S., North R., and Madge, D., "A manufacturing process for GaAs MMICs", Canadian Journal of Appl. Physics, Vol. 65, pp 885-891, 1987.

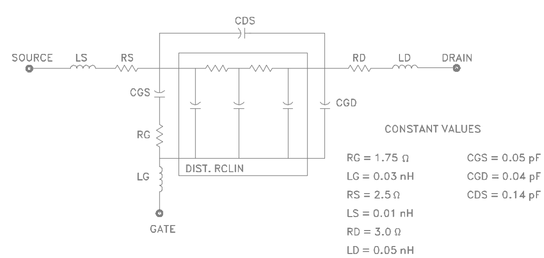
T - ATTENUATOR



ATT (dB)	R1 (Ω)	R2 (Ω)
2	5.73	215.24
4	11.31	104.83
6	16.61	66.93
8	21.53	47.31
10	25.97	35.14
12	29.92	26.81
14	33.37	20.78
22	42.64	7.99

Figure 1 Attenuator Configuration and Attenuation as a Function of Resistances

ZERO-DRAIN BIAS MODEL OF MESFET (COMMON GATE)



VG (% VP)	DISTRIBUTED CAPACITANCE CDIST (pF)	DISTRIBUTED RESISTANCE RDIST (Ω)	ERROR FUNCTION ERRFCT (%)
0 %	0.615	0.211	0.13
10 %	0.5	1.355	0.11
20 %	0.43	2.541	0.09
30 %	0.378	4.578	0.09
40 %	0.337	7.068	0.09
50 %	0.301	10.51	0.1
60 %	0.269	16.6	0.11
70 %	0.240	28.42	0.12
80 %	0.211	53.8	0.14
90 %	0.175	140.2	0.2
100 %	0.135	640	0.6
110 %	0.115	3890	2.0

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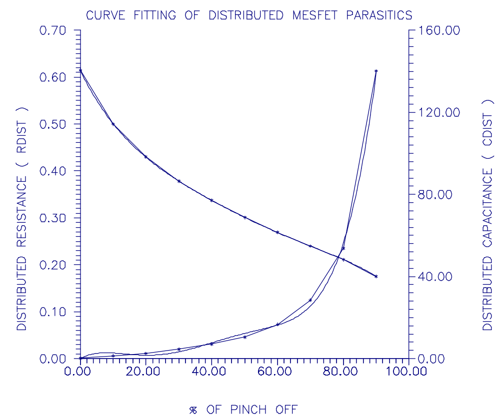
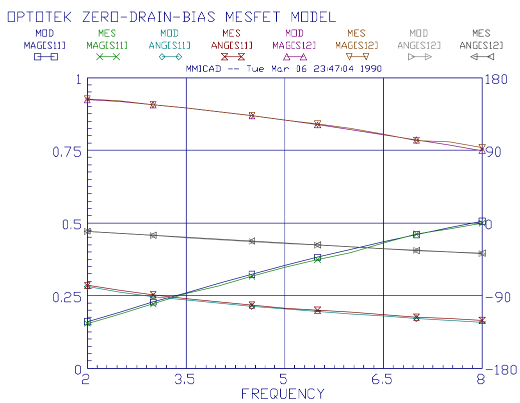
Figure 2 Voltage Dependent Equivalent Circuit of a 600 Micron MESFET






```
! NONLINEAR MESFET MODEL
! OPTOTEK LTD.
!
FILES
\MMICAD\ATTEN\P2VP47.S2P MESCS 101
!
! SET UP THE VOLTAGE CONTROL VARIABLE
VAR
 VC1=20
!
CKT
MODVAR VG=50
! A USER DEFINED MESFET NONLINEAR MODEL
! AS A FUNCION OF GATE BIAS
! RDIST=-.2 + .98VG -.103VG^2 +.0041VG^3
! -6.5E-5VG^4 + 3.65E-7VG^5
! CDIST = .615/(1 + 0.01VG)^1.8
 SRL 1 2 R=2.5 L=0.01
 RCLIN 2 3 4  &
  R={-.2+.98*VG-.103*VG^2+.0041*VG^3-6.5E-5 &
*VG^4+3.65E-7*VG^5 }  &
  C={ .615/(1.+.01*VG)^1.8 } L=1
 SRL 3 5 R=3 L=0.05
 SRL 4 0 R=1.75 L=0.03
 CAP 2 4 C=0.05
 CAP 3 4 C=0.04
 CAP 2 3 C=0.014
!***********************************************
!FMOD IS THE MODEL; THE DEFAULT VALUE OF
!VG IS 50%
 DEF2P 1 5 FMOD ( VG=50 )
!***********************************************
! CONNECT THE MODEL
 FMOD 1 2 0 VG=VC1
 DEF2P 1 2 MOD

!CONNECT THE MESFET
 MESCS 0 2 1 M=1
 DEF2P 1 2 MES

FREQ
 SWEEP 2 8 .5

! DEFINE THE OUTPUT DEFINITIONS.
OUT
 MOD S11 IO
 MES S11 IO
 MOD S12 IO
 MES S12 IO
 MOD MAG[S11] MPP
 MES MAG[S11] MPP
 MOD ANG[S11] MPP R
 MES ANG[S11] MPP R
 MOD MAG[S12] MPP
 MES MAG[S12] MPP
 MOD ANG[S12] MPP R
 MES ANG[S12] MPP R
!
! DEFINE THE OUTPUT GRID
GRID
 MPP 2 8 0 1 R -180 180

!LABEL THE GRAPHS
LABEL
OPTOTEK ZERO-DRAIN-BIAS MESFET MODEL
```

Figure 3 S-Parameter Prediction for a 600 Micron Optotek MESFET

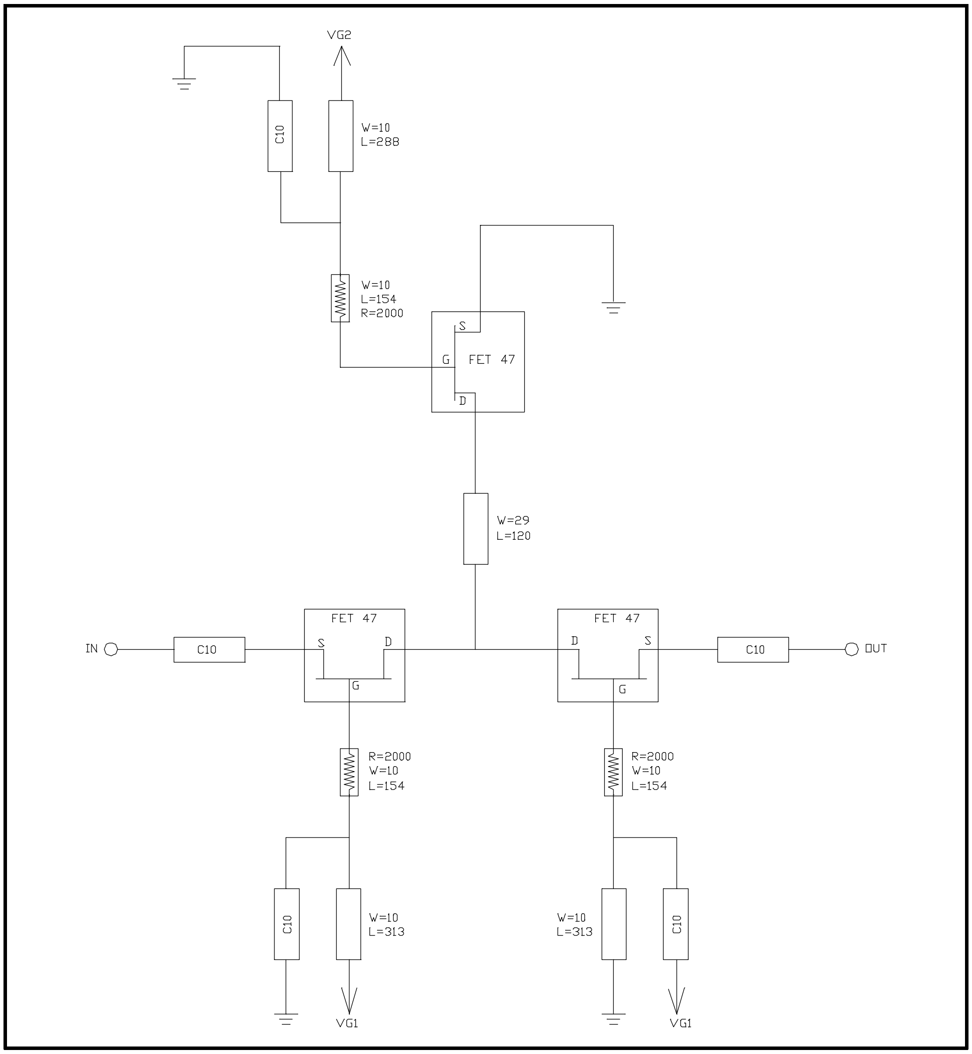
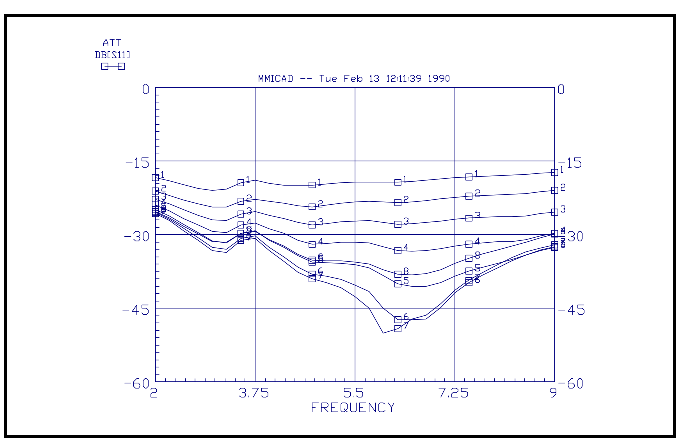
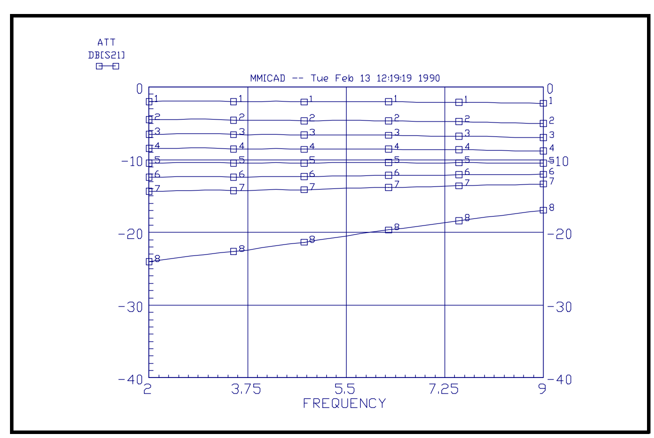


Figure 4 Optimized Electrical Schematic of the Attenuator



(b) S11 vs Frequency



(a) S21 vs Frequency

Figure 5 Simulated Attenuator Performance

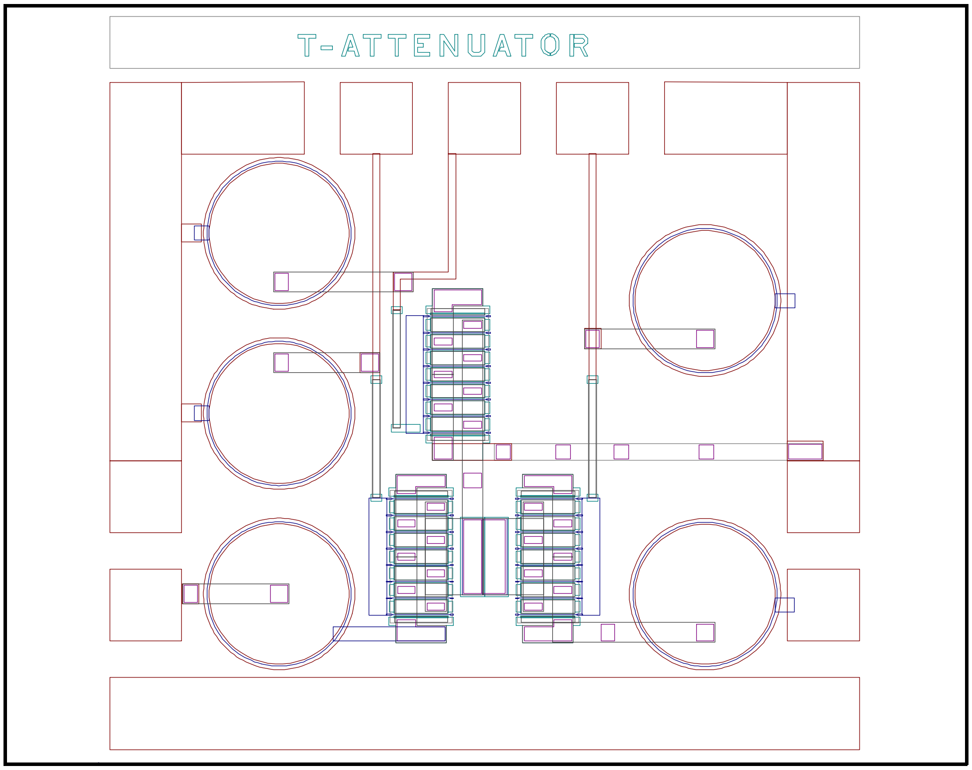


Figure 6 Final Layout

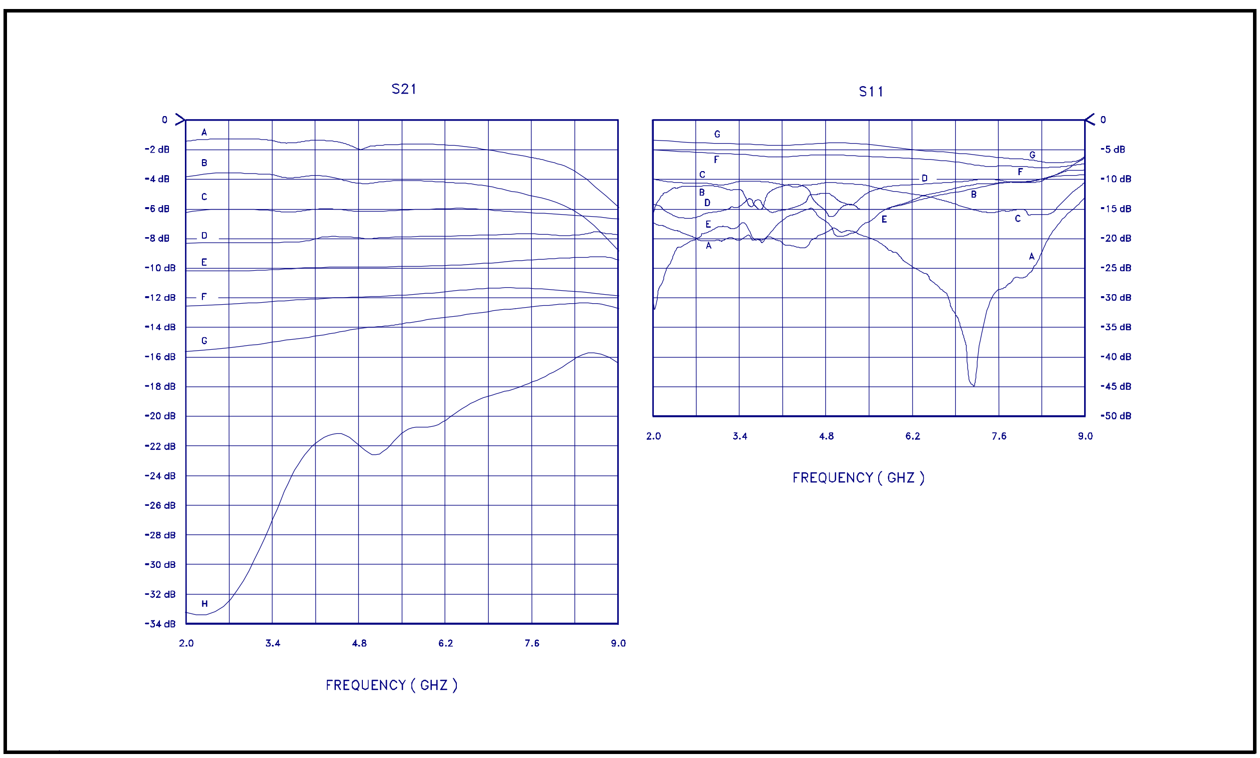


Figure 7   Attenuator Measured Performance